UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/069,754	02/28/2002	Roger W. Whatmore	112113	3781

7590 06/29/2004

Oliff & Berridge
PO Box 19928
Alexandria, VA 22320

EXAMINER	
ALANKO, ANITA KAREN	

ART UNIT	PAPER NUMBER
1765	

DATE MAILED: 06/29/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/069,754	WHATMORE ET AL.	
	Examiner	Art Unit	
	Anita K Alanko	1765	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *5/25/04 amdt*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-4,6-13 and 15-25* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4,6-13 and 15-25* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *25 May 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☒ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☒ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

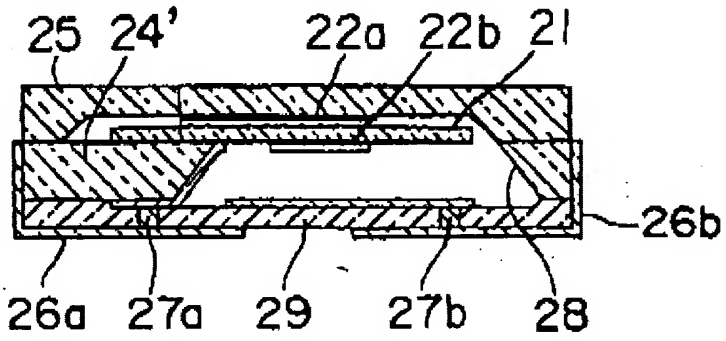
1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Claim Rejections - 35 USC § 103

Claims 1-4, 9-13, 15-17, 21-25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Eda et al (US 5,747,857).

Eda discloses a method for hermetically packaging a bulk acoustic resonator device

FIG. 31D



including the steps of:

providing a first wafer 24' ("holding wafer" Fig. 31D, col.42, lines 21-58, especially lines 51-52) having a first surface and a second surface that face toward opposite directions, with a bulk acoustic resonator device 21 disposed on the first surface (the top surface of 24'), the first wafer further having a cavity 28 formed at a position corresponding to the bulk acoustic resonator device and open at the second surface;

providing a second wafer 25 having a well (col.42, lines 36-37);

providing a third wafer 29 (col.42, lines 52-53);

bonding the second wafer to the first surface of the first wafer and bonding the third wafer to the second surface of the first wafer to form a composite wafer in which the bulk acoustic resonator device of the first wafer is aligned with the wells of the second wafer and sealed by the second wafer (col.42, lines 36-38) and the cavities of the first wafer are sealed by the third wafer (see Fig.31D).

Eda does not explicitly disclose that a plurality of bulk acoustic resonator devices are formed, that the first wafer has a plurality of cavities, or that the second wafer has a plurality of wells. Rather, Eda depicts in Figure 31D that only one of each is formed. Eda also does not disclose to saw to separate the individual devices.

However, in a different embodiment Eda teaches that a plurality of bulk acoustic resonator devices (quartz plate 61 with electrodes 67, 63) can be formed on a first wafer 62, followed by sawing to separate the holding member (col.47, lines 40-41; Fig.35D-35E).

FIG. 35D

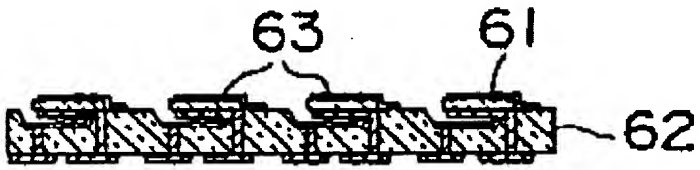


FIG. 35E

The advantage of forming a plurality of devices on a first wafer followed by separation is that they can be mass-produced (col.7, lines 65-67), which is a more efficient method of forming devices.

It would have been obvious to one with ordinary skill in the art to form a plurality of devices with a corresponding plurality of cavities and wells followed by sawing the composite

wafer in the method of Eda because Eda teaches in a different embodiment that forming a plurality of devices on a substrate followed by separation is a useful technique for forming devices and because Eda teaches that an advantage is mass production, which is a more efficient method of forming devices.

As to claim 2, Eda discloses that the bulk acoustic resonator device comprises a piezoelectric layer 21 (quartz) sandwiched between two metal electrodes 22a, 22b (col.42, lines 26-28 and also Fig.31E).

As to claim 3, Eda discloses that holes 27a, 27b are formed in the composite wafer and filled with metal to allow electrical contacts to be made to the bulk acoustic resonator devices (col.42, line 29; since through-holes 16a, 16b of Fig.30 serve the same purpose, col.41, lines 64-66). Eda does not disclose to form the holes by etching. Eda does not disclose how the holes are formed. However, Eda teaches that it is advantageous to use semiconductor techniques in order to enable extremely precise dimensional processing (col.7, lines 51-54). One with ordinary skill in the art readily appreciates that this encompasses using etching to form through-holes.

It would have been obvious to one with ordinary skill in the art to use etching to form the holes in the composite wafer of Eda because Eda teaches that it is advantageous to use semiconductor techniques in order to enable extremely precise dimensional processing, for which etching is a useful technique to form holes.

As to claim 4, Eda discloses to deposit metal layers 26a, 26b (col.42, line 29) on the edges of chips including the bulk acoustic resonator devices in order to allow electrical contacts to be made to the bulk acoustic resonator devices. Eda does not disclose deposition of the metal

layers after separation, however this would have been obvious to one with ordinary skill in the art in order to form a functional device after separation.

As to claim 9, Eda teaches that it is known to use to use a conductive adhesive to bond the substrates together (col.40, lines 23-26), which encompasses using a metal or alloy. It would have been obvious to use a conductive adhesive in the method of Eda because Eda teaches that using conductive adhesives is a known technique for bonding. Using a conductive adhesive inherently uses heat and pressure in order to have effective bonding.

As to claims 10-12, see the rejection of claims 1-2 and Fig.31D. In the embodiment of Figure 31, Eda does not explicitly disclose a dielectric layer over the substrate. However, the substrate comprises a dielectric, and further the direct bonding results in a transitional bonding area between the substrate and the quartz, which encompasses a dielectric layer. Still further, Eda teaches a dielectric layer 8 may be interposed between the substrate and the piezoelectric material 2 (Fig.18A). It would have been obvious to one with ordinary skill in the art to have a dielectric layer over the substrate and under the metal electrode in the method of Eda because Eda teaches that silicon oxide layers are useful for bonding substrates together.

As to claim 13, Eda discloses a top layer 22a which is a conductor.

As to claims 15-17, 21-25, see the corresponding rejection of claims 1-14.

Claims 1-4, 6-13 and 15-25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Eda et al (US 5,747,857) in view of McReynolds (US 5,882,465).

The discussion of Eda from above is repeated here.

As to claim 6, Eda discloses to bond the quartz substrates together (col.39, lines 30+), but does not disclose to use a vacuum.

McReynolds teaches that it is useful to apply a vacuum during bonding in order to have optimal contact (col.5, lines 16-19) and to have a more even application of the pressure forcing the substrates together, which improves efficiency, quality and product yield (col.6, lines 49-61).

It would have been obvious to one with ordinary skill in the art to apply a vacuum as taught by McReynolds in the method of Eda because McReynolds teaches that to do so provides for optimal contact and for a more even application of the pressure forcing the substrates together, which improves efficiency, quality and product yield.

As to claim 7, Eda discloses to use anodic bonding (col.40, lines 4-15) with a silicate bonding layer (quartz). Eda does not disclose to employ a borosilicate bonding layer.

McReynolds teaches that quartz and borosilicate glasses are useful, alternative materials for one another (col.4, lines 25-37) and that quartz typically bonds at higher temperatures than borosilicate glass.

It would have been obvious to one with ordinary skill in the art to use borosilicate as a bonding layer in the method of Eda because McReynolds teaches that it is a known useful alternate silicate glass for quartz, and because McReynolds teaches that it has a lower bonding temperatures, which improves product yield.

As to claim 8, Eda discloses to use heating (col.40, lines 4-8), but does not disclose to use pressure.

McReynolds teaches that a useful bonding technique includes applying heat in combination with pressure (col.4, lines 19-22).

It would have been obvious to one with ordinary skill in the art to use heat and pressure during bonding in the method of Eda because McReynolds teaches that it is a useful technique for bonding.

As to claims 18-20, see the corresponding rejection of claims 6-8.

Claims 1-4, 9-13. 15-17, 21-25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Eda et al (US 5,747,857) in view of Kurle et al (US 6,106,735).

The discussion of Eda from above is repeated here.

As to claim 1, Eda not explicitly disclose that a plurality of bulk acoustic resonator devices are formed, that the first wafer has a plurality of cavities, or that the second wafer has a plurality of wells. Rather, Eda depicts in Figure 31D that only one of each is formed. Eda also does not disclose to saw to separate the individual devices.

Kurle teaches a method for protecting sensors or arrangements from external influences by forming an airtight seal (col.4, lines 30-35). Electrical elements 2 are provided in a first wafer 1 and bonded to a second wafer 3. The second wafer has a plurality of wells (created by webs 4). During bonding, electrical elements 2 are aligned with the wells of the second wafer (col.2, lines 56-62, Fig. 1D). After bonding, the electrical elements 2 are separated into individual devices (col.3, lines 10-13) by sawing.

It would have been obvious to one with ordinary skill in the art to form a plurality of devices with a corresponding plurality of cavities and wells followed by sawing the composite wafer in the method of Eda because Kurle teaches that forming devices, bonding wafers and then

sawing to separate devices is a useful technique for forming devices and because Eda teaches that an advantage is mass production, which is a more efficient method of forming devices.

Claims 1-4, 6-13, 15-25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Eda et al (US 5,747,857) in view of McReynolds (US 5,882,465) (as applied to claims 6-8 and 18-20) and Kurle et al (US 6,106,735) (as applied to claims 1 and 15).

The discussion of modified Eda from above is repeated here.

Response to Amendment

The objection to the drawings is withdrawn. The drawing correction filed 5/25/04 is approved.

The 102 rejection over Tomita is withdrawn. Applicant's point is well taken that Tomita does not disclose disposing a plurality of bulk acoustic resonator devices on the first surface of a first wafer.

The rejection of claims 1, 3-5, 7-14 under 35 U.S.C. 103(a) as being unpatentable over Ella (US 6,081,171) in view of Kurle et al (US 6,106,735) and the rejection of claims 1-14 under 35 U.S.C. 103(a) as being unpatentable over Ella (US 6,081,171) in view of Kurle et al (US 6,106,735) and Sparks et al (US 6,062,461). Applicant's point is well taken that there is no suggestion to bond a third wafer to the second surface of the first wafer and thereby have the cavities of the first wafer sealed by the third wafer.

The rejection of claims 1, 3-14 under 35 U.S.C. 103(a) as being unpatentable over the combination of Kurtz et al (US 5,891,751), Lakdawala et al (1998 IEEE) and Sparks et al (US

6,062,461). Applicant's point is well taken that there is no suggestion to bond a third wafer to the second surface of the first wafer and thereby have the cavities of the first wafer sealed by the third wafer. Rather, Kurtz uses a sealing member to seal the cavities.

Claims 1-25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Eda et al (US 5,747,857) in various combinations with McReynolds (US 5,882,465) and Kurle et al (US 6,106,735).

Response to Arguments

Applicant's arguments filed 5/25/04 have been fully considered and are persuasive as noted above. The claims are rejected over newly cited Eda et al.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Wright (Fig.8b, Fig.9) is cited to show a method of packaging bulk acoustic resonators.

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period

will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Anita K Alanko whose telephone number is 571-272-1458. The examiner can normally be reached on Mon,Tues & Fri: 8:30 am-5 pm; Wed&Thurs:10 am-2 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nadine Norton can be reached on 571-272-1465. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Anita K. Alanko

Anita K Alanko
Primary Examiner
Art Unit 1765